WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

a first conductivity type well area formed in a surface area of the semiconductor substrate;

a plurality of element isolation areas formed in the well area;

a second conductivity type semiconductor layer formed at a first area of the well area which is isolated by the element isolation areas, the semiconductor layer configuring a first electrode of a capacitor; and

a first conductivity type low resistance area provided at a base portion of the well area, the low resistance area having a resistive value lower than that of the well area.

2. The device according to claim 1, further comprising a first conductivity type semiconductor layer formed in a second area of the well area which is isolated by the element isolation areas, the first conductivity type semiconductor layer configuring a second electrode of the capacitor.

3. The device according to claim 1, wherein the low resistance area is not in contact with a depletion layer of a junction portion between the semiconductor layer and the well area and is in contact with the element isolation areas.

4. The device according to claim 2, wherein the low resistance area is situated from the first conductivity type semiconductor layer to the second conductivity type semiconductor layer at a base portion of the well area.

5. The device according to claim 1, wherein the impurity concentration of the low resistance area is set to above 2 times that of the well area.

6. The device according to claim 5, wherein the impurity concentration of the low resistance area is set to above 1×10^{18} cm^{-3}.

7. A semiconductor device comprising:

a semiconductor substrate;

a first conductivity type well area formed in a surface area of the semiconductor substrate;

a plurality of element isolation areas formed in the well area;

an MOS transistor formed in a first area of the well which is isolated by the element isolation areas; and

a first conductivity type provided at a base portion of the well area and having a resistive value lower than that of the well area.

8. The device according to claim 7, further comprising a first conductivity type semiconductor layer formed in a second area of the well area which is isolated by the element isolation areas.

9. The device according to claim 7, wherein the low resistance area is not in contact with a depletion layer of a junction portion between source/drain regions of the MOS transistor and is in contact with the element isolation areas.

10. The device according to claim 8, wherein the low resistance area is situated from the first conductivity type semiconductor layer to the second conductivity type semiconductor layer at a base portion of the well area.

11. The device according to claim 7, wherein the impurity concentration of the low resistance area is set to above 2 times that of the well area.

12. The device according to claim 11, wherein the impurity concentration of the low resistance area is set to above 1×10^{18} cm^{-3}.

13. A semiconductor device comprising:

a semiconductor substrate;

a first conductivity type well area formed in a surface area of the semiconductor substrate;

a plurality of element isolation areas formed in the well area;

a second conductivity type base layer formed on the well area which is isolated by the element isolation areas, the well area configuring a first electrode of a bipolar transistor;

a first conductivity type second electrode formed

on the base layer; and

a first conductivity type low resistance area provided at the base portion of the well area, the low resistance area having a resistive value lower than that of the well area.

14. The device according to claim 13, wherein the low resistance area is not in contact with a depletion layer of a junction portion of the bipolar transistor and is in contact with the element isolation areas.

15. The device according to claim 13, further comprising:

a first conductivity type semiconductor layer formed in a second area of the well area which is isolated by the element isolation areas, the low resistance area being situated from the first conductivity type semiconductor layer to a second conductivity type semiconductor layer in the base portion of the well area.

16. A semiconductor device comprising:

a semiconductor substrate;

a first well area formed in a surface area of the semiconductor substrate;

a second well area formed in a surface area of the semiconductor substrate;

an analog circuit formed in the first well area;

a digital circuit formed in the second well area; and

a first conductivity type low resistance area provided at a base portion of the first well area, the first conductivity type low resistance area having a resistive value lower than that of the first well area.

17. The device according to claim 16, wherein the impurity concentration of the low resistance area is set to above 2 times that of the well area.

18. The device according to claim 16, wherein the impurity concentration of the low resistance area is set to above 1×10^{18} cm^{-3}.

19. The device according to claim 17, wherein the impurity concentration of the first well area where the analog circuit is provided is set to be higher than that of the second well area where the digital circuit is provided.